IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC., Plaintiff, v. FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC., and FAIRCHILD SEMICONDUCTOR CORPORATION, Defendants.	)	**REDACTED PUBLIC VERSION** C.A. No. 04-1371-JJF

OPENING BRIEF IN SUPPORT OF DEFENDANTS' MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT OF U.S. PATENT NO. 4,811,075

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I. INTRODUCTION.

The undisputed evidence establishes that Power Integrations unequivocally disclaimed coverage of DMOS devices during prosecution of the '075 Patent. As a matter of law, Power Integrations cannot read the claims of the '075 Patent on the disavowed DMOS devices.

The defining feature of a DMOS (short for "double-diffused MOS") structure is a source diffusion region formed completely within a channel diffusion region, rather than directly within the semiconductor substrate. Hence the term "double-diffused". The overwhelming evidence demonstrates that such structures where known as DMOS to those of skill in the art in 1987, when the application for the '075 Patent was filed, in 1988, when Power Integrations disclaimed coverage of DMOS devices during prosecution of that patent, and today, when Power Integrations is trying to read the '075 Patent on the disclaimed DMOS devices. A DMOS device illustrating this characteristic structure is shown in Fig. 53(a) of Sze, *Physics of Semiconductor Devices*, 2nd Ed. P. 489, which is intrinsic evidence to the prosecution history of the '075 Patent. In Fig. 53(a) the channel diffusion region is labeled p-shield and the source diffusion region, which is contained entirely within that channel diffusion region is labeled n+-source:

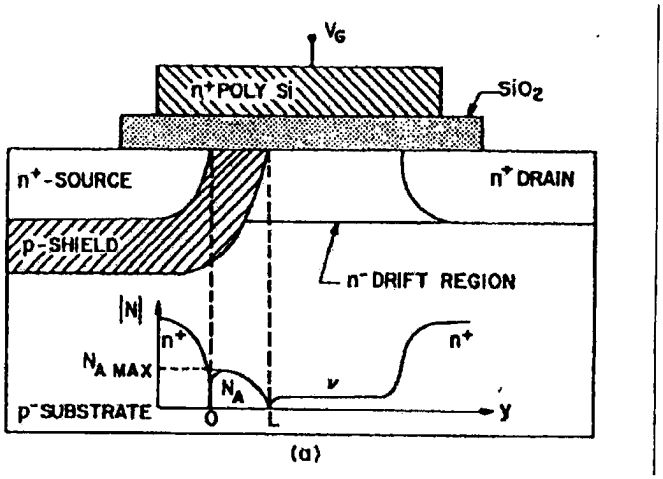

Fig. 53(a) of Sze, *Physics of Semiconductor Devices*, 2nd Ed. P. 489

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Thus, as a matter of law, Power Integrations should not be permitted to read the claims of its '075 Patent on the accused structures.

Power Integrations attempts to avoid this inevitable result by arguing that Fairchild's devices are not truly DMOS structures because

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This argument ignores the overwhelming evidence that Power Integrations disavowed DMOS devices and not a limited subset of DMOS devices made by a particular process. Power Integrations never mentioned a particular process for making a DMOS structure anywhere in its prosecution history. In the 1980's, as there are today, many methods existed that could be used to fabricate DMOS structures. Power Integrations also ignores the fact that both the '075 Patent, as well as the prior art Power Integrations was seeking to overcome, claimed device structures and any method of fabricating the devices.

For the same reasons, the claims of the '075 Patent do not read on Fairchild's DMOS devices. During prosecution, Power Integrations amended its claims to avoid DMOS devices in the prior art and specifically relied on the characteristic structural feature of DMOS devices – having a source diffusion region formed in a doped channel region rather than directly within the substrate – to distinguish its claims. In particular, Power Integrations added a requirement to its claims that the source diffusion region must be formed "within the substrate." If Power Integrations is permitted to read this "within the substrate" claim limitation on Fairchild's DMOS devices by including the P Body channel diffusion region as part of the "substrate," it would ensnare the very prior art Power Integrations argued to overcome. Accordingly, as a matter of law, Power Integrations cannot read the claims of the '075 Patent on the accused products and Fairchild is entitled to summary judgment of non-infringement.

II. BACKGROUND.

A. Power Integrations Has Only Asserted Claims 1 And 5 Of The '075 Patent.

Power Integrations, Inc. ("Power Integrations") has accused Fairchild Semiconductor International, Inc. and Fairchild Semiconductor Corporation (collectively "Fairchild") of infringing two claims of U.S. Patent No. 4,811,075 (the "'075 Patent") – independent claim 1 and dependant claim 5. A copy of the '075 Patent is attached as Exhibit A.[1] Since claim 5 depends from – and incorporates all of the limitations of – claim 1, if the accused Fairchild devices do not infringe claim 1 they cannot, as a matter of law, infringe claim 5.

B. Fairchild's Proprietary DMOS Transistors.

Power Integrations accuses 35 Fairchild products ("accused Fairchild products") of infringing claims 1 and 5 of the '075 Patent.[2] In particular, Power Integrations asserts that Fairchild's proprietary high voltage DMOS transistors, which are incorporated into each of the accused products, infringe claim 1 of the '075 Patent. Claim 1 is directed towards a specific MOS transistor structure. Exh. A. Power Integrations further asserts that the combination of Fairchild's DMOS transistors with low voltage circuitry on a single chip infringes claim 5, which depends for its purported novelty on the specific MOS structure of claim 1. *Id.*

Fairchild devoted substantial resources to the development of its own DMOS transistors. Exh. B, Jeon Depo. Vol. II, 63:12-64:13.

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Despite Power Integrations' failure to mark any of its own products with the '075 patent number, Fairchild located the '075 Patent during its search. *Id.*, 19:11-20:8 and 66:5-15.

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[1] For the convenience of the Court, Fairchild has highlighted the relevant passages of certain exhibits in yellow. In all such cases, the highlighting has been added by Fairchild and is not part of the original exhibit.

[2] FAN7601, FSD200, FSD200B, FSD210, FSD210B, FSD211, FSD500, FSDH321, FSDH321L, FSDH565, FSDH0165, FSDH0265RL, FSDH0265RN, FSDH0265RLB, FSDH0265RNB, FSDL321, FSDL0165RL, FSDL0165RN, FSDL0365RL, FSDL0365RN, FSDL0365RNB, FSDM311, FSDM0265RL, FSDM0265RLB, FSDM0265RN, FSDM0265RNB, FSDM0365R, FSDM0365RL, FSDM0365RLB, FSDM0365RN, FSDM0365RNB, FSDM0565, FSDM0565R, FSDM07653, and FSDM07652R.

In analyzing the '075 Patent, Fairchild observed that the drawings and claims were directed towards a conventional MOS structure rather than the DMOS structure Fairchild was developing. REDACTED This was readily apparent to Fairchild's engineers as neither the drawings nor claims included a diffused channel region surrounding the source diffusion region, which is characteristic of DMOS structures:

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REDACTED *also* '075 Patent, Figure 1, which shows the source contact pocket (21) directly within the substrate (11).

Nonetheless, Fairchild obtained the file history for the '075 Patent in order to verify its understanding of the scope of the patent. It is undisputed that in reviewing the file history, Fairchild learned that Power Integrations had expressly disclaimed coverage of DMOS devices. REDACTED It is also undisputed that Fairchild engineers relied on Power Integrations' disclaimer to conclude that Fairchild's planned DMOS structure avoided the invention of the '075 Patent and that they could proceed with developing Fairchild's own DMOS transistor without fear of trampling on Power Integrations' intellectual property:

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The two Fairchild transistor structures that are accused of infringing the '075 Patent are

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[3] This figure was relied upon by Power Integrations expert Mr. Shields in his Opening Expert Report to describe the basis for Power Integrations' assertion of infringement and thus is not in dispute. *See* Exh. C, Shields' Opening Expert Report, Exh. E.

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C, Shields' Opening Expert Report, p. 12.

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Id., Shields' Opening Expert Report at Ex. E.

C. The '075 Patent Claims A Specific MOS Transistor Structure.

Power Integrations '075 Patent describes and claims a specific structure for a high voltage MOS transistor that incorporates a layer of material of opposite conductivity on top of a portion of an extended drain region. The only purportedly novel feature of Power Integrations' claims was the addition of this top layer of opposite conductivity type material, as it is undisputed that high voltage MOS transistors, including those with extended drain regions, were known at the time of the '075 Patent's invention. Power Integrations also admitted in the '075 Patent that the prior art included combining high voltage MOS transistors with low voltage logic circuitry on the same integrated circuit:

> Self isolation technology is used for making high voltage MOS devices, particularly ***integrated high voltage devices in combination with low voltage control logic on the same chip.*** The voltage is sustained by an offset gate, ***as a lightly doped extended drain region is used.*** Such devices can be considered as an IGFET or MOSFET in series with a single sided JFET.

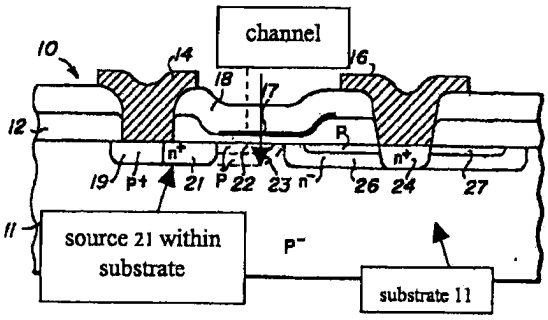
'075 Patent, 1:16-22 (emphasis added). Power Integrations admitted this prior art in its patent, and thus cannot dispute these facts during litigation.

D. The Patentee Of The '075 Patent Disclaimed Coverage Of DMOS devices.

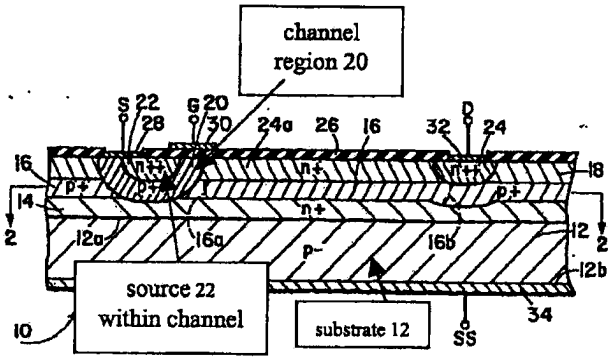
During prosecution, the Examiner determined that the purportedly novel element of the MOS structure claimed in the '075 Patent – incorporating a top layer of material of opposite conductivity type on top of an extended drain region – was included in a prior art DMOS structure disclosed in U.S. Patent No. 4,626,879 ("Colak"), a copy of which is attached as Exhibit D. The Examiner thus rejected the asserted claims of the '075 Patent as anticipated by Colak. *See* Exh. E, '075 Pros. Hist., FCS0000160.

In response, Power Integrations never directly challenged the prior art rejection but instead argued its invention was limited to ***conventional MOS structures*** and amended its claims to expressly exclude ***DMOS structures***. Power Integrations clearly narrowed its claims. In

particular, Power Integrations added a requirement that the source diffusion region (referred to as a "pocket" in the patent) be "within the substrate" in order to distinguish DMOS structures. The parties agree that in DMOS structures the source is formed entirely within a more heavily doped channel region, rather than directly within the substrate as in a conventional MOS structure. Exh. C, Shields Report, p.8; Exh. B, Jeon Depo. vol. II, 67:19-25. This fundamental difference between DMOS and conventional MOS structures, ***which Power Integrations relied upon to distinguish its claims***, is readily apparent from comparing the MOS structure shown in Figure 1 of the '075 Patent (which shows source contact pocket (21) directly within substrate (11)) with the DMOS structure shown in Figure 1 of the Colak patent (which shows source region (22) within channel region (20)).



'075 MOS Transistor
(Exh A, '075 Patent, Fig. 1)



DMOS structure
(Exh. D, Colak Patent, Fig. 1)

This distinguishing feature of DMOS structures is also described in Sze, the seminal reference for semiconductor devices in the mid-1980's and part of the intrinsic record cited by the Examiner. As explained in Sze:

> Figure 53a shows the ***DMOS (double-diffused MOS)*** structure, where the channel length L is determined by the higher rate of diffusion of the p-dopant (e.g., boron), compared to the n^+-dopant (e.g., phosphorus) of the source.

Exh. F, Sze, at 489 (footnote omitted) (emphasis added). The p dopant refers to the channel diffusion region and the n+ dopant refers to the source diffusion region. As shown in Figure 53a, the n+ dopant source diffusion region is entirely within the p dopant channel diffusion region (referred to as "p-shield in the figure).

In addition to amending its claims to exclude the characteristic feature of DMOS structures, Power Integrations expressly relinquished coverage of DMOS devices in its statements to the Examiner. In particular, in response to the Examiner's initial rejection, Power Integrations stated:

> Claim 19 [which issued as claim 1] also provides for a pair of laterally spaced source and drain contact pockets within the substrate as is customary for conventional MOS transistors ***and is thus, distinguished from DMOS devices*** which require a higher threshold voltage.

See Exh. E, '075 Pros. Hist., FCS0000172 (underlined emphasis in original, italicized emphasis added).[5] Power Integrations reiterated its explicit disavowal of DMOS devices in response to a second rejection based on Colak:

> [C]laim 19 [which issued as claim 1] ***is limited to a MOS or MOSFET structure, while Colak shows a D-MOS device.***

See id., '075 Pros. Hist., FCS0000187 (emphasis added). In light of Power Integrations' repeated, clear and unambiguous statements that its patent did not cover DMOS devices, the Examiner allowed the pending claims, which issued as the '075 Patent.

Power Integrations' express disavowals of DMOS devices, as well as its claim amendments directed at explicitly excluding DMOS structures, cannot be disputed as those facts are set forth unambiguously in the intrinsic record of the '075 Patent.

III. ARGUMENT.

A. Summary Judgment Standard.

Summary judgment is properly granted when no genuine and disputed issues of material fact remain, and when, viewing the evidence most favorably to the non-moving party, the movant is clearly entitled to prevail as a matter of law. *Celotex Corp. v. Catrett*, 477 U.S. 317, 322-23 (1986) ("In our view, the plain language of Rule 56(c) mandates the entry of summary judgment, after adequate time for discovery and upon motion, against a party who fails to make a showing

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[5] *See also* Declaration of Dr. Peter Gwozdz in Support of Defendants' Partial Motion for Summary Judgment of Non-Infringement of U.S. Patent No. 4,811,075 ("Gwozdz Decl."), Exh. B, ¶¶ 27-37 (explaining that because the channel region of the DMOS structure is more heavily doped than the substrate of a conventional MOS device it requires a higher threshold voltage).

sufficient to establish the existence of an element essential to that party's case, and on which that party will bear the burden of proof at trial.") The Federal Circuit has emphasized that: "[s]ummary judgment is appropriate in a patent case as in any other." *Barmag Barmer Maschinenfabrik AG v. Murata Machinery, Ltd.*, 731 F.2d 831, 835 (Fed. Cir., 1984).

In a patent case, "[s]ince the ultimate burden of proving infringement rests with the patentee, an accused infringer seeking summary judgment of non-infringement may meet its initial responsibility either by providing evidence that would preclude a finding of infringement, or by showing that the evidence on file fails to establish a material issue of fact essential to the patentees' case." *Novartis v. Ben Venue Labs*, 271 F.3d 1043, 1046 (Fed. Cir. 2001). Fairchild has done both. First, Fairchild has provided evidence that precludes a finding of infringement, specifically that: (1) Power Integrations disclaimed coverage of DMOS devices during prosecution; and (2) the accused devices are DMOS structures, as that term was understood in the art at all relevant times. Second, the undisputed evidence presented by Fairchild demonstrates

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and thus that Power Integrations will be unable to establish that any of the accused devices practice each and every element of any asserted claim.

Power Integrations cannot refute these material facts and will be unable to meet its burden of showing that there is a genuine issue for trial. *Novartis*, 271 F.3d at 1046 ("Once the movant has made [its] showing, the burden shifts to the nonmovant to designate specific facts showing that there is a genuine issue for trial."). Based on the evidence produced in this case, a rational finder of fact could come to but one conclusion: none of the accused products infringe the '075 Patent. Accordingly, Fairchild is entitled to summary judgment.[6]

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[6] According to Power Integrations expert, Mr. Shields, Power Integrations is only asserting literal infringement and not infringement under the doctrine of equivalents. Exh. C, Shields' Report, ¶ 11. This is because prosecution history estoppel bars Power Integrations from expanding the scope of its claims to reach the accused DMOS structures. Power Integrations narrowed the literal scope of its claims by amending them to require that the source and drain contact regions are "within the substrate." *See Pioneer Magnetics, Inc. v. Micro Linear Corp.*, 330 F.3d 1352, 1356 (Fed. Cir. 2003). Power Integrations did so for a substantial reason related to patentability – to overcome prior art DMOS devices – and thus surrendered all territory between the original claim and the amended claim limitation. *See Festo Corp. v. Shoketsu*

B. Power Integrations Disclaimed DMOS devices During Prosecution Of The '075 Patent.

Power Integrations cannot deny that it disclaimed coverage of DMOS devices during prosecution in order to avoid the prior art. In fact, Power Integrations stated unequivocally on two separate occasions – both times in response to rejections by the Examiner – that the claims of the '075 Patent do not cover DMOS devices. *See* Exh. E, '075 Pros. History, FCS0000172 ("Claim 19 [which issued as claim 1]... is... distinguished from DMOS devices") and FCS0000187 ("[C]laim 19 [which issued as claim 1] is limited to a MOS or MOSFET structure, while [the prior art] shows a D-MOS device.") Power Integrations also amended its claims precisely to avoid claiming DMOS structures in which the source diffusion region is completely within a channel diffusion region, rather than directly within the substrate. *Supra* at II.D.

Power Integrations cannot go back and change the scope of its disclaimer in order to now capture Fairchild's DMOS structures. The law requires that Power Integrations' statements during prosecution limiting the scope of its claims to conventional MOS structures must be given full effect. "The prosecution history limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution." *Southwall Tech., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995). "The purpose of consulting the prosecution history in construing a claim is to exclude any interpretation that was disclaimed during prosecution." *Chimie v. PPG Indus.*, 402 F.3d 1371, 1384 (Fed. Cir. 2005) (internal quotes omitted).

1. "DMOS" Is Defined As A Double Diffused *Structure* In The Intrinsic Evidence.

The only argument Power Integrations makes in the face of the indisputable evidence of its disavowal of DMOS devices is that the disclaimer should be limited

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Shields Report, p. 7. This argument should be rejected as a matter of law, because it is without any support in the intrinsic record. Bluntly, Power Integrations expert attempts to re-write the prosecution history to include a new definition of

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Kinzoku Kogyo Kabushiki Co., 535 U.S. 722, 740 (U.S. 2002); *Pioneer*, 330 F.3d at 1356-57.

DMOS never presented to the Patent Office.

To begin, Power Integrations was claiming – and distinguishing – DMOS devices, not a particular method or process for fabricating those structures as Power Integrations now does. The intrinsic record likewise describes a double-diffused structure; it never specified the method for fabricating the two diffusions. *See* Exh. D, Colak Patent, 1:12-13, Figure 1; Exh. F, Sze, p. 489; *supra* at I, II.D. As Power Integrations has admitted, and as is clear from the intrinsic record, the defining feature of the disclaimed DMOS devices is a double diffused structure in which one diffusion forms a channel diffusion region and a second diffusion forms a source diffusion region that is completely within that channel diffusion region. *Supra* at II.D. It was precisely this double-diffused structural feature that Power Integrations relied upon to distinguish its claimed MOS structure from prior art DMOS structures, and which must now give meaning to Power Integrations' disavowal. *See supra* at II.D.

2. The Extrinsic Evidence Does Not Support Power Integrations' Limitation Of Its Disavowal To A Particular Process.

Even if the Court were to consider the extrinsic evidence, as a matter of law DMOS should still be defined as a structure in which the source diffusion region is completely within a channel diffusion region. *See Markman v. Westview Instruments, Inc.*, 517 U.S. 370 (1996) (construction of a patent is a question of law to be decided by the Court). The overwhelming evidence establishes that DMOS was understood in 1987, as it is today, as denoting a ***double-diffused structure***, which could be formed by many different methods.

a. The Inventor's own testimony refutes Power Integrations' assertion that "DMOS" required diffusion through the same opening.

Dr. Eklund agrees with Fairchild that in 1987 it was understood that "DMOS" was a structure that could be formed through different processes:[7]

[7] The Federal Circuit has held that inventor testimony is extrinsic evidence. Here, Fairchild cites the deposition testimony of Klas H. Eklund, the sole inventor named on the '075 Patent, only to rebut Power Integrations' assertion that in 1988 "DMOS" required REDACTED REDACTED

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Exh. G, Deposition of Klas Eklund, 98:15-99:14. Dr. Eklund admits that it was well-known in the art that a REDACTED for a structure to be DMOS. He agrees that back at the relevant time, those skilled in the art generally knew that REDACTED REDACTED He agrees that, at the time the '075 Patent was filed, a definition of DMOS as REDACTED was another valid definition. The inventor's own testimony thus rebuts Power Integrations' assertion that "DMOS" required a particular process in which diffusion occurred REDACTED in 1987. Power Integrations ignores its own inventor's testimony.

b. <u>There were many known methods for fabricating DMOS structures in 1987.</u>

The evidence consistently demonstrates that those of ordinary skill in the art would have understood that DMOS structures could be fabricated in various different ways. Gwozdz Decl, ¶ 5, Exh. B, ¶¶ 32-34 and Exh A, ¶¶ 17-25. In fact, the intrinsic Sze reference describes other methods for fabricating DMOS structures. *See* Exh. F (Sze), and Gwozdz Decl., ¶ 6.

The extrinsic evidence provides further methods. For example, a 1986 article entitled "A Novel CMOS-Compatible High-Voltage Transistor Structure", by Zahir Parpia et. Al., IEEE

Transactions on Electron Devices, ED-33, Dec. 1986, page 1948 ("Parpia") describes making a DMOS structure through a different process. Gwozdz Decl., Exh. C. Figure 1 of the Parpia article shows a DMOS structure with the source entirely within a more heavily doped channel region rather than directly within the substrate. The Parpia article explains that instead of diffusing both the N+ source and the P body through the same opening, the N+ source and the P body are diffused through different openings. Parpia teaches separate diffusions using separate masks, to achieve a DMOS structure. Power Integrations is thus wrong when it claims that in 1987 there was only one process for forming DMOS structures.

3. Power Integrations Cannot Create A Genuine Issue Of Fact By Citing To Expert Testimony.

Power Integrations improperly relies on the testimony of its expert Mr. Shields for its assertion that it only disclaimed a particular process for fabricating DMOS structures and not the structures themselves. As the Federal Circuit has recognized, such expert testimony is irrelevant in determining the scope of Power Integrations' claims. The public has the right to rely on the intrinsic record, or in the very least, information that was publicly available at the relevant time:[8]

> Claim interpretation, as a question of pure law, is amenable to summary judgment and disagreement over the meaning of a term within a claim does not necessarily create a genuine issue of material fact. Any other rule would be unfair to competitors who must be able to rely on the patent documents themselves without consideration of expert opinion that then does not even exist, in ascertaining the scope of a patentee's right to exclude.

Southwall Tech., Inc. v. Cardinal IG Co., 54 F.3d 1570, 1578 (Fed. Cir. 1995) (internal citations omitted); *see also* D.I. 166, pp. 11-12. In the instant case, as discussed above the intrinsic and extrinsic evidence available to the public at the relevant time overwhelmingly demonstrates that those of skill in the art understood DMOS to refer to double diffused ***structures*** in which the source diffusion region is completely within a channel diffusion region. Power Integrations'

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[8] Power Integrations' citation to the Penguin Dictionary also does not create a genuine issue of material fact as it was likewise unavailable in 1987. Moreover, the Penguin Dictionary simply provides one example of a DMOS process available for fabricating DMOS structures in 1988 – by successive diffusions though the same opening in the oxide layer. Indeed, it does not even mention the other process for manufacturing DMOS structures (using the same edge of a mask layer) that Power Integrations' expert admits was available at the time. *See also* D.I. 166 (Defendants' Answering Claim Construction Brief), pp. 12-13.

unsupported, litigation-induced disagreement over the meaning of DMOS does not create a genuine issue of material fact. *See Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 247-48 (1986) ("the mere existence of some alleged factual dispute" is not enough).

4. The Law Entitles Fairchild To Rely Upon Power Integrations' Disavowal Of DMOS.

It is fundamentally unfair for Power Integrations to change its disclaimer almost 20 years later to recapture Fairchild's DMOS devices since Fairchild specifically relied on Power Integrations' disavowal. The Federal Circuit has held that Fairchild is entitled to rely upon Power Integrations' statements during prosecution to ascertain the scope of the '075 Patent's invention. *See Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) ("[C]ompetitors are entitled to review the public record, apply the established rules of claim construction, ascertain the scope of the patentee's claimed invention and, thus, design around the claimed invention.") Power Integrations cannot be allowed to first argue to the Examiner that the '075 Patent does not cover DMOS devices in order to get the claims allowed, only to turn around decades later and accuse Fairchild's DMOS devices of infringing those very same claims. *Spring Windows Fashions LP v. Novo Indus., L.P.*, 323 F.3d 989, 995 (Fed. Cir. 2003) ("A patentee may not state during prosecution that the claims do not cover a particular device and then change position and later sue a party who makes that same device for infringement."); *Southwall*, 54 F.3d at 1576 ("Claims may not be construed one way in order to obtain their allowance and in a different way against accused infringers."). As a matter of law, Power Integrations infringement claims must fail.

The undisputed evidence demonstrates that Fairchild (i) reviewed the file history for the '075 Patent well prior to the lawsuit, (ii) determined based on Power Integrations' statements that the '075 Patent did not apply to DMOS devices, and (iii) relied on those statements to proceed to develop, manufacture, market and sell the accused DMOS devices. *See supra* at II.B. As a matter of law, these facts alone should preclude a finding that the accused devices infringe the

'075 Patent and the Court should grant summary judgment of Power Integrations' infringement claims in Fairchild's favor.

C. The Accused Fairchild Products Are DMOS, And Therefore Not Covered By The Claims Of The '075 Patent.

The relevant structure of the accused devices is not in dispute for purposes of this motion; Fairchild assumes Power Integrations' asserted structure for its devices. Power Integrations does not deny that the accused Fairchild devices have a double-diffused structure consisting of REDACTED

REDACTED In fact, Power Integrations expert, Mr. Shields, describes REDACTED

. *Supra* at II.B. As described above, this double-diffused structure is characteristic of the DMOS devices disclaimed by Power Integrations during prosecution of the '075 Patent. Thus, as a matter of law, Power Integrations cannot read the claims of its '075 Patent on the accused structures.

1. REDACTED

Power Integrations attempts to avoid non-infringement by arguing that Fairchild's devices are not the disclaimed DMOS devices because during fabrication

Although there are

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According to Mr. Shields,

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This is absurd. The intervening steps are irrelevant to the '075 Patent, which claims a device structure rather than a method or process for device fabrication. Neither the claims nor the specification of the '075 Patent specify, or even describe, any process, method or steps for fabricating MOS devices. Surely Power Integrations would never agree that someone could avoid infringement of its patented MOS structure simply by using REDACTED

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Likewise, intervening processing steps should not limit the scope of Power Integrations' disavowal of DMOS devices. The prior art Power Integrations was seeking to overcome was a DMOS structure, not a particular process for making that structure, and thus the method by which the structure was made is irrelevant.

2. REDACTED

Power Integrations tries to recapture the disavowed DMOS devices by arguing that Fairchild's devices are not DMOS structures because of the type of REDACTED According to Mr. Shields' "made-for-litigation" test, Fairchild's devices are not DMOS because were the REDACTED Exh. C, Shields Expert p. 8. This is not a valid method for determining whether a device is a DMOS structure. Exh. H, Gwozdz Supplemental Expert Report. To begin, no such test has ever esixted outside of this litigation and was never used during the relevant time period in 1987. Indeed, Mr. Shields could not cite to any support for his "test" in the prosecution history or other intrinsic or extrinsic record because none exists. Exh. C, Shields Expert Report, p. 8. Second, obviously REDACTED REDACTED would significantly impact the performance of the transistors, or Fairchild would not have gone through the additional effort of REDACTED to form a DMOS transistor.

Rather, the evidence overwhelmingly demonstrates that a person of ordinary skill in the art in the mid 1980's would not use Mr. Shield's "made-for-litigation" test to determine whether a device was a DMOS structure. In fact, prior art from as early as 1982 directly contradicts Mr. Shields "made-for-litigation" test and shows that devices with the characteristic DMOS structure of REDACTED were considered to be DMOS devices even though

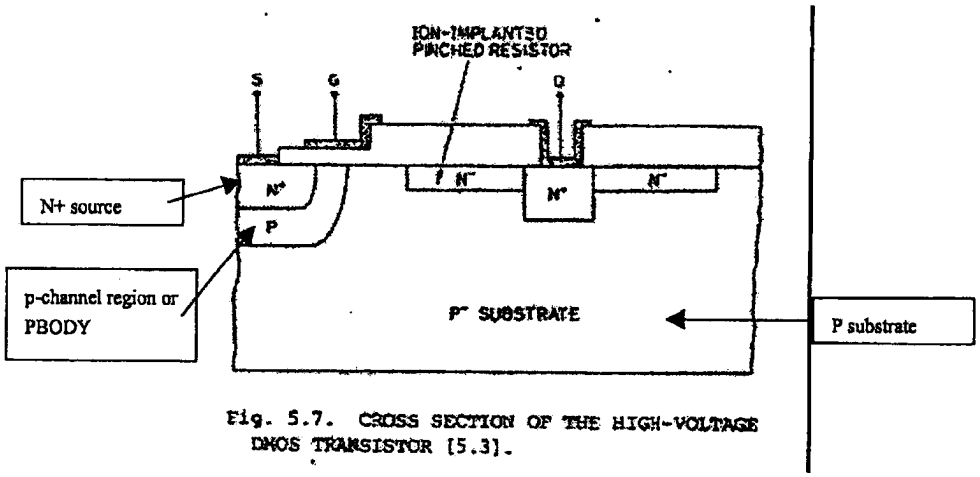


Fig. 5.7. CROSS SECTION OF THE HIGH-VOLTAGE DMOS TRANSISTOR [5.3].

For example, the above figure from a publicly available 1982 dissertation by Shi-Chung Sun rebuts Power Integrations litigation-induced claim. Exh. J, "Physics and Technology of Power MOSFETs", FCS1689399 (Exhibit 12 to the Shields Deposition). This figure shows a DMOS transistor fabricated in a P- substrate. Removal of REDACTED from the depicted device leaves an n-p-n junction series. Thus, REDACTED this 1982 prior art DMOS device, it too would flunk Mr. Shields' "made-for-litigation" test. Mr. Shields' test would thus exclude this known DMOS device .

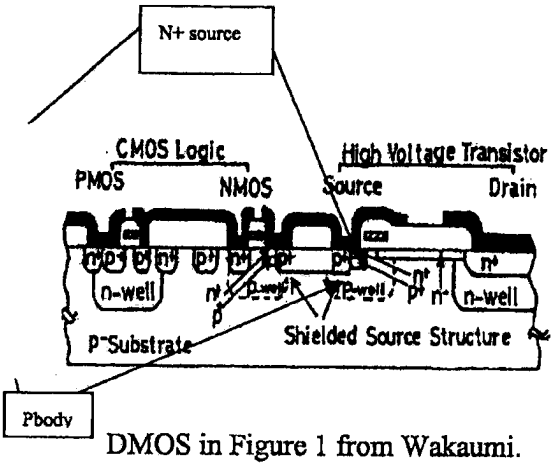
Another article referenced in the inventor's own notebook disclosed a DMOS structure fabricated on a P type substrate which would also fail Mr. Shields' "test." This article is entitled "A Highly Reliable 16 Output High Voltage NMOS/CMOS Logic IC With Shielded Source Structure," by H. Wakaumi, T. Suzuki, M. Saito and H. Sakuma ("Wakaumi"), and is attached as Exhibit K. Although the article did not specifically refer to the structure in Figure 1 of Wakaumi as "DMOS," REDACTED

REDACTED Exh. I, Eklund notebook, KE00003. REDACTED

REDACTED *Id.* The Wakaumi article, combined with Dr. Eklund's notes, further demonstrate that one of ordinary skill would not have used Mr. Shields' test to determine whether a device was a DMOS structure. Gwozdz Decl., ¶8.

The Fairchild DMOS structure is remarkably similar to the Sun and Wakaumi DMOS structures in this regard. All have a P body in a P substrate. All have an M+ source within the P body and not completely within the substrate. All have a channel within the body. Compare the following picture of the accused Fairchild DMOS structure with the DMOS shown in Figure 1 from Wakaumi (shown side by side below) and also with the above Figure 5.7 from Sun:

REDACTED



Accused Fairchild DMOS structure.

DMOS in Figure 1 from Wakaumi. Referenced in Eklund Notebook

D. Power Integrations Cannot Show That The Accused Fairchild Products Practice Each And Every Element Of Any Claim Of The '075 Patent.

Power Integrations will be unable to show that the accused Fairchild products infringe either of the two asserted claims (1 and 5) of the '075 Patent. Claim 5 of the '075 Patent is dependent upon claim 1, and thus incorporates each and every element of claim 1. As shown below, the accused products do not include the claimed "pair of laterally spaced pockets... within the substrate."

Claim 1 of the '075 Patent requires "[a] pair of laterally spaced pockets of semiconductor material of a second conductivity type within the substrate and adjoining the substrate surface." '075 Patent. This pair of laterally spaced pockets refers to the source and drain diffusion regions of the claimed MOS structure.

As discussed above, it is undisputed that the source diffusion region of the accused Fairchild products is contained entirely within the P Body channel diffusion region, rather than

within the substrate. *See supra* at II.B. Likewise, it is undisputed that REDACTED REDACTED REDACTED Exh. C, Shields' Opening Expert Report, Exh. E. Accordingly, no trier of fact reasonably could conclude that the claims of the '075 Patent read on the accused products.

Power Integrations again tries to avoid this inevitable result, this time by arguing that the REDACTED REDACTED This argument must be rejected as a matter of law. Power Integrations added the requirement that the source and drain pockets be formed "within the substrate" during prosecution to distinguish the prior art Colak structure.[9] *See supra* II.D. The source "pocket" of the Colak structure is contained within a channel diffusion region, as in the accused products, rather than "within the substrate." Similarly, the drain "pocket" of Colak is contained within epitaxial layers (similar to the N well of the accused products) rather than "within the substrate." If the term "substrate" was construed to include REDACTED REDACTED the claims of the '075 Patent would no longer be distinguished from the prior art Colak structure.[10] Accordingly, Power Integrations' attempt to read this claim limitation on the accused products is clearly incorrect and does not create a genuine issue of material fact.

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[9] Power Integrations admitted at the Claim Construction Hearing that it had distinguished Colak on the basis that the source and drain diffusion regions were not "within the substrate":

> Very hard for you to get a handle on this without reading through the prosecution history or the clerk reading through it. But what you will find is ***[Power Integrations] did disclaim a piece of Colak... as not being within the substrate.*** Again, we're not here to tell you otherwise.

Exh. H, Claim Construction Hearing Transcript, 88:11-17 (emphasis added).

[10] In essence, Power Integrations is attempting to make an equivalence argument, which it is not permitted to do because it narrowed its claims during prosecution for this very reason. *See Festo*, 535 U.S. at 740.

IV. CONCLUSION.

For the foregoing reasons, Fairchild respectfully requests that the Court grant summary judgment in its favor on Power Integrations' claims of infringement of the '075 Patent.

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Dated: March 17, 2006

CERTIFICATE OF SERVICE

I hereby certify that on the 23rd day of March, 2006, the attached **REDACTED PUBLIC VERSION OF OPENING BRIEF IN SUPPORT OF DEFENDANTS' MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT OF U.S. PATENT NO. 4,811,075** was served upon the below-named counsel of record at the address and in the manner indicated:

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